AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to Figure 16. Prior art Figure 16 is amended to change reference numeral "90" to reference numeral --92-- to clarify that the uppermost layer on the right-hand side of the figure is a connecting lead. In addition, reference numerals 50, 52, 54 and 56 are changed to 50', 52', 54' and 56' consistent with the rest of the Figure 16 and as disclosed on page 35, lines 19-26 of the application as filed.

REMARKS

Initially, Applicants would like to thank Examiner Nadav for granting an interview and for his time spent in the interview.

The application has been amended to place it in condition for allowance at the time of the next Official Action.

The specification is amended to make editorial changes so that the drawings are consistent with the specification.

Prior art Figure 16 is amended to change reference numeral "90" to reference numeral --92-- to clarify that the uppermost layer on the right-hand side of the figure is a connecting lead. In addition, reference numerals 50, 52, 54 and 56 are changed to 50', 52', 54' and 56' consistent with the rest of the Figure 16 and as disclosed on page 35, lines 19-26 of the application as filed. The above noted changes are the only changes and are believed not to introduce new matter.

Claims 1-8 and 24-29 were previously pending in the application. New claim 30 is added. Therefore, claims 1-8 and 24-30 are presented for consideration.

Claims 1-8 are rejected as anticipated by applicants' disclosed prior art Figures 16 and 17 and the related text on page 1-5 and 35-38. This rejection is respectfully traversed.

Claim 1 is amended as suggested at the interview to recite a first metal wiring layer that is subjected to a provisional yield-rate test. Claim 1 is also amended as

suggested at the interview to recite a second metal wiring layer formed on the first metal wiring layer when the wafer passes the provisional yield-rate test.

As set forth at the interview, prior art Fig. 16 of the present application shows and page 37, lines 21-26 of the present application disclose a conventional semi-finished semiconductor device including a basic wiring arrangement section 16' and a custom-purpose wiring arrangement section 48'. These two wiring sections 16' and 48' are the only wiring sections and are both formed before any yield rate test is performed.

Based on the interview summary indicating that an amendment to claim 1 as above would overcome the rejection and in view of the above noted differences, reconsideration and withdrawal of the rejection are respectfully requested.

Claims 2-8 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art.

Claims 24-29 are rejected as unpatentable over applicants' disclosed prior art in view of HAQ 6,245,677 or ROSTOKER et al. 6,418,353. This rejection is respectfully traversed.

Claims 24-28 recite the steps of forming a first metal wiring layer then performing a yield-rate test and then forming a second metal wiring layer on the first metal wiring layer. Claims 24-28 are believed patentable over applicants' disclosed prior art

at least for the reasons set forth above with respect to claims 1-8.

Both HAQ and ROSTOKER are only cited for the teaching of performing a yield rate test on a finished product. Neither HAQ nor ROSTOKER teaches the steps of forming a first metal wiring layer then performing a yield-rate test and then forming a second metal wiring layer on the first metal wiring layer.

The above noted features are missing from each of the references, are absent from the combination and thus would not have been obvious to one having ordinary skill in the art.

Claim 29 recites the steps of forming a first metal wiring layer. Claim 29 further recites performing a provisional yield-rate test to determine whether the first metal wiring layer is acceptable or unacceptable and then forming a second metal wiring layer on the first metal wiring layer as a finished semiconductor device.

As set forth above, the proposed combination of references does not teach or suggest these steps and thus claim 29 is also believed patentable over the cited art.

New claim 30 recites the step of depositing and patterning a metal layer to form at least one second metal wiring layer over at least one first metal wiring layer when a wafer passes a provisional yield-rate test.

Applicants' disclosed prior art teaches at page 36, lines 21-25, a yield-rate test performed on the semi-finished

semiconductor device that includes both layers 16' and 48'. Thereafter, the uppermost circuit pattern is rearranged and customized in accordance with a customer's request, as disclosed on page 36, lines 27-31.

Accordingly, the conventional method forms both the first and second wiring arrangements, and then rearranges the second wiring arrangement when the wafer passes a yield-rate test. Applicants' disclosed prior art does not teach depositing a second metal wiring layer over a first metal wiring layer when the wafer passes a provisional yield-rate test as recited.

As set forth above, HAQ and ROSTOKER are only cited for the teaching of performing a yield rate test on a finished product. Neither HAQ nor ROSTOKER teach or suggest the step of depositing and patterning a metal layer to form at least one second metal wiring layer over at least one first metal wiring layer when a wafer passes a provisional yield-rate test as recited.

Accordingly, new claim 30 is believed patentable over the art of record.

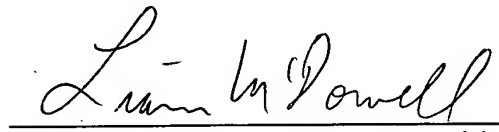
In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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Appendix:

The Appendix includes the following item:

- Replacement Sheet for Figure 16 of the drawings